Abstracts

A monolithic 2.8 V, 3.2 W silicon bipolar power amplifier with 54% PAE at 900 MHz

A. Heinz, W. Simburger, H.-D. Wohlmuth, P. Weger, W. Wilhelm, R. Gabl and K. Aufinger. "A monolithic 2.8 V, 3.2 W silicon bipolar power amplifier with 54% PAE at 900 MHz." 2000 Radio Frequency Integrated Circuits (RFIC) Symposium 00. (2000 [RFIC]): 117-120.

This work presents a balanced two-stage monolithic power amplifier in Si bipolar technology for 0.8-1 GHz. On-chip transformers are used as input-baluns as well as for interstage matching. A closed-loop bias circuit is introduced to diminish break-down effects and increase the maximum usable supply voltage. The chip is operating from 2.8 V to 4.5 V. At 2.8 V the output power is 3.2 W with a power-added efficiency of 54%. The maximum output power of 7.7 W with an efficiency of 57% is achieved at 4.5 V supply voltage. The small-signal gain is 38 dB.

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